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09/889,380	07/16/2001	Masashi Nakamura	450106-02849	3746

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EXAMINER	
MA, JOHNNY	

ART UNIT	PAPER NUMBER
2623	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/889,380	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Johnny Ma	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6-14 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-14 and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 2, 6-14, and 18-24 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7-9, 13, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chimoto et al. (US 5,838,383 of record) in further view of Vorenkamp et al. (US 2002/0047942 A1), Proehl et al. (US 2005/0204389 A1), and Foster et al. (US 6,654,835 B1).

As to claim 1, note the Chimoto et al. reference that discloses a multimedia television receiver and method of booting the same. The claimed "a plurality of digital signal processing blocks including at least a signal processing block for decoding data streams" is met by "[a]s FIG.1 shows, the television receiver 301 comprises a bus 302, an NTSC decoder module 303, a digital broadcast-signal receiving module 304, a depacket processing module 305, a digital cable module 306, an MPEG video module 304, and an MPEG audio module 308. The bus 302 connects the modules 302 to 308, one another. The receiver 301 further comprises...a CPU 313" (Chimoto 7:50-60) wherein "[t]he MPEG video module 307 decodes the video data stream into image data" (Chimoto 7:50-60).

Note, the Chimoto et al. reference teaches "[t]he CPU 313 executes this program to control the other components of the receiver 301. The CPU 313 can set parameters in the modules 303 to 308 and change the parameters whenever necessary" (7:61-66) wherein the control to set parameters [commands] is transmitted through the bus 302 as illustrated in Figure 1. However, the Chimoto et al. reference does not specifically teach the modules , each of said plurality of digital signal processing blocks, having a general-purpose Central Processing Unit. Now note the Vorenkamp et al. reference that teaches the claimed ""each of said digital processing blocks having a general-purpose Central Processing Unit" wherein in the digital single processing block 8305 DSP techniques are utilized so that conventional analog circuit functions are fabricated with digital signal processing circuitry, DSP circuit elements advantageously allow digital programmability of the parameters of each circuit such that a high degree of flexibility in using and programming the digital module is possible such that input signals formatted to various standards may be accommodated (Vorenkamp [0844]). The DSP processor, inherent to the Vorenkamp et al. DSP circuit element in order to process signals or instructions, is equivalent to the claimed general-purpose Central Processing Unit, the DSP processor is a general purpose process in that modifying the DSP parameters results in the ability to change the type/purpose of processing performed. Therefore, the examiner submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Chimoto et al. modules with the Vorenkamp DSP modules "to allow digital programmability of the parameters of each circuitry such that a high degree of flexibility in using and programming the digital module is possible" (Vorenkamp [0844]).

The claimed "wherein said Central Processing Units of each of said digital signal processing blocks interprets and executes said command" is met by the Chimoto et al. and Vorenkamp et al. combination teaching modules with general purpose Central Processing Units as discussed above wherein, for example, "[t]he CPU 313 supplies prescribed parameters through the DMA device 312 and the bus 302 to the digital broadcast-signal receiving module 304, the depacket processing module 305, the PEG video module 307, and the MPEG audio module 308. Once these parameters are set in the modules 304, 305, 307 and 308, these modules are made to receive and process BS signals" (Chimoto 9:27-34).

Note the Chimoto et al. reference discloses "[t]he CPU 313 [host processing block] executes this program to control the other components of the receiver 301. The CPU 313 can set parameters in the modules 303 to 308 and change the parameters whenever necessary" (Chimoto 7:61-65). However, the Chimoto et al. reference is silent as to the type of command that is sent being high layer.

Now note the Proehl et al. reference that teaches the use of high layer commands (Proehl [0052]). Therefore, the examiner submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Chimoto et al. commands with the Proehl et al. high layer commands to provide system flexibility by obviating the need for specialized drivers to communicate with different components.

The claimed "and that is not on real time basis' is met by "the DMA device 312 controls the transfer of data through the bus 302" wherein it is inherent that the command not be transmitted on a real time basis when data is in the process of being transferred on the bus in order to avoid transfer errors. The claimed "a bus for connecting said host processing black and said plurality

of digital signal processing blocks for transferring said command and for transferring said data of streams" is met by bus 302 connected to a plurality of modules 303-308 [digital signal processing blocks] and the CPU 313 [host processing block] as illustrated in Figure 1 (Chimoto) wherein "[t]he CPU 313 supplies prescribed parameters through the DMA device 312 and the bus 302 to the digital broadcast-signal receiving module 304..." (Chimoto 9:27-34) and "[i]n the receiver 301, the receiving module 304 selects the BS signals of the channel designated by the remote control data supplied from the remote-controller 309 and converts them into a stream of bits. The stream of bits is supplied to the bus 302" (Chimoto 9:35-50).

The claimed "wherein [...] streams of video data and streams of audio data [...] are [...] transmitted at high speed" is met by the transfer of video and audio data over bus 302 (Chimoto 8:1-25). Furthermore, the Chimoto et al. reference teaches data transfer over bus 302 is controlled by the DMA device 312 (Chimoto 8:27-36). However, the Chimoto et al. reference is silent as to the method employed by the DMA device to control data transfers. Now note the Foster et al. reference that teaches high bandwidth data transfer employing a multi-mode, shared line buffer. The claimed assignment of priorities for data transmission at a high speed is met by the assignment of priorities to modules for access to the shared bus (Foster 6:20-27). Therefore, the examiner submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Chimoto DMA controlling of data transfers over the system bus with the Foster et al. module bus access based on prioritization for the purpose of facilitating the sharing of the bus resource between the different modules and to ensure that, during bus resource conflicts, more important data is processed timely.

As to claim 7, the claimed "wherein the data of streams contains video data and / or audio data" is met by "[t]he MPEG data stream consists of a video data stream and an audio data stream" (Chimoto 9:46-47).

As to claim 8, the claimed "wherein the video data and / or the audio data has been compressed" is met by "the MPEG data stream" (Chimoto 9:46-47) wherein MPEG is a compression scheme.

As to claim 9, the claimed "wherein said bus is a general-purpose bus" is met by bus 302 as illustrated in Figure 1. The claimed "wherein each block connected to said bus can be added or substituted" is met by "the modules 303 to 308 can be removed form the housing of the receiver 301. Therefore, the modules 303 to 308 can easily be replaced by other modules to change the functions the receiver 301 can perform. Furthermore, the receiver 302 may have extra module receptacles to incorporate additional modules" (Chimoto 10:54-59).

As to claims 13 and 19-21, please see rejections of claims 1 and 7-9 respectively.

4. Claims 6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chimoto et al. (US 5,838,383 of record) in further view of Vorenkamp et al. (US 2002/0047942 A1), Proehl et al. (US 2005/0204389 A1), Foster et al. (US 6,654,835 B1), and Humpleman et al. (US 6,198,479 B1 of record).

As to claim 6, note the Chimoto et al. reference discloses "[t]he CPU 313 executes this program to control the other components of the receiver 301" (Chimoto 7:61-63) and "the receiver 302 may have extra module receptacles to incorporate additional modules" (Chimoto 10:58-59). However, the Chimoto reference does not specifically disclose "wherein the command is described and embedded in a script of hypertext, wherein the hypertext is

interpreted by a browser and a picture for operating the extension function is displayed, and wherein a command corresponding to the function is embedded and displayed in the picture for operating the extension function." Now note the Humpleman et al. reference that discloses home network, browser based, command and control. The claimed "wherein the command is described and embedded in a script of hypertext, wherein the hypertext is interpreted by a browser and a picture for operating the extension function is displayed" is met by "[t]he browser based DTV 102 receives the HTML files from the home devices over the home network 100 using the HTTP protocol. Each HTML file contains specific control and command information for a respective home device. The HTML files enable the browser based DTV 102 to graphically display control and command information to a user for a particular home device" (Humpleman 6:60-66). The claimed "and wherein a command corresponding to the function is embedded and displayed in the picture for operating the extension function" is met by the embedding of commands in the picture "708" as illustrated in Figure 11. Therefore, the examiner submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Chimoto receiver with extra module receptacles with the Humpleman et al. controlling of other devices for the purpose extending the upgrade functionality of the receiver and to allow a user to easily control diverse devices in their home with a single remote control.

As to claim 18, please see rejection of claim 6.

5. Claims 2, 10-12, 14, and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chimoto et al. (US 5,838,383 of record) in further view of Vorenkamp et al. (US

2002/0047942 A1), Proehl et al. (US 2005/0204389 A1), Foster et al. (US 6,654,835 B1), and Trovato et al. (US 6,469,742 B1 of record).

As to claim 2, the claimed "wherein said plurality of digital signal processing blocks include at least a front end block for processing a received signal of a digital broadcast" is met by digital broadcast-signal receiving module 304 and digital cable module 306" (Chimoto 7:50-60). However, the Chimoto et al. reference does not disclose the claimed "wherein one of said plurality of digital signal processing blocks is a plug-in interface block for connecting external hardware." Now note the Trovato et al. reference that teaches consumer electronic devices with adaptable upgrade capability. The claimed "wherein one of said plurality of digital signal processing blocks is a plug-in interface block for connecting external hardware" is met by modules may include communication modules (radio frequency, infrared, serial/parallel ports, etc.). Therefore, the examiner submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Chimoto and Vorenkamp digital signal processing blocks (modules) with the Trovato et al. communication modules for the purpose of providing a device that can readily accept and take advantage of new software/hardware (Trovato 3:43-63).

As to claim 10, the claimed "wherein when each block connected to said bus is added or substituted, software for operating the added or substituted block is automatically installed." Note the Chimoto et al. reference discloses "[t]he main memory stores a control program, The CPU 313 executes this program to control the other components of the receiver 301" (Chimoto 7:61-65) and "the modules 303 to 308 can be removed form the housing of the receiver 301. Therefore, the modules 303 to 308 can easily be replaced by other modules to change the

functions the receiver 301 can perform. Furthermore, the receiver 302 may have extra module receptacles to incorporate additional modules" (Chimoto 10:54-59). However, the Chimoto reference is silent as to installing software to control the new modules. Now note the Trovato et al. reference that discloses consumer electronic devices with adaptable upgrade capability. The claimed "software for operating the added or substituted block is automatically installed" is met by "[o]nce new modules are identified an automatic upgrade may be provided" (Trovato 4:45-61). Therefore, the examiner submits that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Chimoto adding/substituting modules on the bus with the Trovato et al. automatic installation of corresponding software for the purpose of providing software/driver needs without requiring user interaction and without unnecessarily storing a plurality of different device drivers (Trovato 5:27-34).

As to claim 11, the claimed "wherein software for operating the added or substituted block is stored in a memory there of" is met by the Chimoto et al. and Trovato et al. combination as discussed above wherein "[m]odules 16 may include device drivers and protocols for interfacing with CPU 12 stored in memory 17" (Trovato 4:20-21).
The claimed "wherein when the block is added or substituted, the software stored in the memory is installed" is also met by the Chimoto et al. and Trovato et al. combination as discussed above wherein "[o]nce new modules are identified an automatic upgrade may be provided [/installed]" (Trovato 4:50-51; 5:9-11).

As to claim 12, the claimed "wherein when each block connected to said bus is added or substituted, a service center is accessed through a telephone line, software for operating the added or substituted block is downloaded from the service center through the telephone line, and

the downloaded software is installed" is met by the Chimoto et al. and Trovato et al. combination as discussed above wherein "system 100 includes a remote station 101. Remote station 101 includes a transmitter 102 for transmitting upgrade information to a plurality of devices 10. Transmission of upgraded information may be delivered by a...telephone network...Remote station 101 may further include a receiver 106 for receiving and handling transmission requests from devices 10 which need upgrade or new software pursuant to hardware changes as described above" (Trovato 5:35-49) wherein "[u]pon receiving the appropriate driver(s) or information, device 10 is upgraded and the registry of modules is updated in operating system 20" (Trovato 5:9-11).

As to claim 14, please see rejection of claim 2.

As to claim 22, please see rejection of claim 10.

As to claim 23, please see rejection of claim 11.

As to claim 24, please see rejection of claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johnny Ma whose telephone number is (571) 272-7351. The examiner can normally be reached on 8:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on (571) 272-7331. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jm

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